AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An apparatus, comprising:

interpolator circuitry to proportion amplitude contributions of reference clock phases;

phase control circuitry coupled with said interpolator circuitry to adjust ~~a~~the proportion of the amplitude contributions based upon an interrelated control signal, the phase control circuitry to provide the interpolation circuitry with a bias current that varies according to the interrelated control signal;

degenerative mesh circuitry coupled with said phase control circuitry to ~~determine proportions of a~~control the variation of the bias current based upon a substantially differential portion of the interrelated control signal and another control signal; and

output circuitry coupled with said interpolator circuitry to generate a phase of an interpolated clock signal based upon a combination of the amplitude contributions.

Claims 2-5 (Canceled).

6.(Previously Presented) The apparatus of claim 1, wherein the degenerative mesh circuitry comprises substantially equivalent impedances coupled between more than two circuits of said phase control circuitry.

7.(Currently Amended) The apparatus of claim 1, wherein said interpolator circuitry comprises a current-steering mechanism to generate a current from a particular one of the reference clock phases with ~~a~~the bias current.

8.(Currently Amended) The apparatus of claim 1, wherein said interpolator circuitry comprises a differential current-steering mechanism to steer ~~a~~the bias current between two conductive paths based upon a substantially differential signal of the reference clock phases.

9.(Currently Amended) The apparatus of claim 1, wherein said interpolator circuitry comprises a differential current-steering mechanism to determine an amplitude contribution of a particular one of the reference clock phases based upon an amplitude of ~~a~~the bias current pulled through the differential current-steering mechanism.

10.(Currently Amended) The apparatus of claim 1, wherein said phase control circuitry comprises circuitry coupled with said interpolator circuitry to adjust an amplitude of ~~a~~the bias current based upon the interrelated control signal.

11.(Currently Amended) The apparatus of ~~claim 1~~claim 7, wherein said phase control circuitry comprises a conductive path coupled between a current source and ~~a~~the current-steering mechanism to adjust ~~a~~the bias current in substantially linear proportion to a change in the interrelated control signal.

12.(Currently Amended) The apparatus of claim 1, wherein said phase control circuitry comprises a differential amplifier having an output for ~~a~~the bias current coupled to said interpolator circuitry.

13.(Original) The apparatus of claim 1, wherein said output circuitry comprises circuitry to combine amplitude contributions of a first phase and a second phase of the reference clock phases.

14.(Original) The apparatus of claim 1, wherein said output circuitry comprises filtering circuitry to filter the amplitude contributions of the reference clock phases.

15.(Original) The apparatus of claim 14, wherein the filtering circuitry comprises circuitry to integrate the amplitude contributions of the reference clock phases.

16.(Original) The apparatus of claim 14, wherein the filtering circuitry comprises circuitry to differentiate the amplitude contributions of the reference clock phases.

17. (Previously Presented) A method, comprising:
receiving more than one phase of a reference clock signal;

receiving an interrelated ramping control voltage signal associated with a first phase and a second phase of the more than one phase of the reference clock signal;

proportioning an amplitude contribution of the first phase and an amplitude contribution of the second phase, based upon the interrelated control signal; and

combining the amplitude contributions of the first phase and the second phase based upon said proportioning, to generate a phase of an interpolated clock signal with a substantially analog transition.

18. (Original) The method of claim 17, further comprising filtering a combination of the amplitude contributions of at least one phase of the more than one phase to output the interpolated clock signal.

19. (Original) The method of claim 17, further comprising determining an output based upon a substantially differential portion of the interrelated control signal and another control signal.

20. (Original) The method of claim 17, wherein said receiving more than one phase of a reference clock signal comprises receiving the first phase and the second phase, wherein the first phase is less than 180 degrees from the second phase.

21. (Original) The method of claim 20, wherein said receiving an interrelated control signal comprises receiving a first interrelated control signal associated with the first phase and a second interrelated control signal associated with the second phase, wherein the first interrelated control signal increases in amplitude at a substantially equivalent rate that the second interrelated control signal decreases in amplitude.

22. (Original) The method of claim 17, wherein said proportioning comprises increasing the amplitude contribution of the first phase at substantially the same rate as decreasing the amplitude contribution of the second phase.

23. (Original) The method of claim 17, wherein said combining comprises combining the amplitude contributions of the first phase and the second phase, wherein

amplitude contributions of the first phase and the second phase are proportioned based upon a voltage of the interrelated control signal.

24. (Currently Amended) A system, comprising:

a phase controller to provide ~~an~~N interrelated control ~~signal~~signals, N being three or more;

clock circuitry to provide reference clock phases; and

a phase interpolator coupled to said clock circuitry, comprising

interpolator circuitry to proportion amplitude contributions of the reference clock phases as a function of the N current signals;

phase control circuitry coupled with the interpolator circuitry to adjust the proportion of amplitude contributions based upon the N interrelated control ~~signal~~signals, the phase control circuitry having N amplifier circuits that adjust the N current signals in accordance with the N interrelated control signals;

~~degenerative~~ mesh circuitry coupled between ~~a first circuit of said phase control circuitry and a second circuit of said phase control circuitry to degenerate an amplifier that comprises the first circuit, the second circuit, and the degenerative mesh circuitry~~the N amplifier circuits to degenerate the N amplifier circuits; and

output circuitry coupled with the interpolator circuitry to generate a phase of an interpolated clock signal based upon a combination of the amplitude contributions.

25. Canceled.

26. (Original) The system of claim 24, wherein said interpolator circuitry comprises a differential current-steering mechanism to determine an amplitude contribution of a particular reference clock phase of the reference clock phases based upon an amplitude of a bias current pulled through the differential current-steering mechanism.

27. (Currently Amended) The system of ~~claim 24~~claim 26, wherein said phase control circuitry comprises a conductive path coupled between a current source and ~~a~~the

current-steering mechanism to adjust ~~a~~the bias current in substantially linear proportion to a change in a particular one of the N interrelated control ~~signal~~signals.

Claims 28-30 (Canceled).

31. (Currently Amended) An apparatus, comprising:

interpolator circuitry to proportion amplitude contributions of reference clock phases;

phase control circuitry coupled with said interpolator circuitry to adjust ~~a~~the proportion of the amplitude contributions based upon an interrelated control signal;

current circuitry coupled with said phase control circuitry to provide a static bias current;

degenerative mesh circuitry coupled with said phase control circuitry to apportion the static bias current based upon the interrelated control signal; and

output circuitry coupled with said interpolator circuitry to generate a phase of an interpolated clock signal based upon a combination of the amplitude contributions.

32. (Previously Presented) The apparatus of claim 31, wherein said interpolator circuitry comprises a current-steering mechanism to generate a current from a particular one of the reference clock phases with a bias current.

33. (Previously Presented) The apparatus of claim 31, wherein said interpolator circuitry comprises a differential current-steering mechanism to steer a bias current between two conductive paths based upon a substantially differential signal of the reference clock phases.

34. (Previously Presented) The apparatus of claim 31, wherein said interpolator circuitry comprises a differential current-steering mechanism to determine an amplitude contribution of a particular one of the reference clock phases based upon an amplitude of a bias current pulled through the differential current-steering mechanism.

35. (Currently Amended) The apparatus of ~~claim 33~~claim 34, wherein said phase control circuitry comprises a conductive path coupled between a current source and ~~a~~the current-steering mechanism to adjust ~~a~~the bias current in substantially linear proportion to a change in the interrelated control signal.

36. (Previously Presented) The apparatus of claim 31, wherein said phase control circuitry comprises a conductive path coupled between a current source and a current-steering mechanism to adjust a bias current in substantially linear proportion to a change in the interrelated control signal.

37. (Previously Presented) The apparatus of claim 31, wherein said output circuitry comprises circuitry to combine amplitude contributions of a first phase and a second phase of the reference clock phases.